

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for reducing total code size, comprising the steps of:

determining a latency between a defining instruction and a using instruction and
inserting a NOP field into at least one of said defining and using instruction, wherein said NOP field is inserted at an end of said using instruction.

2. (Original) The method of claim 1, wherein said NOP field is inserted into said defining instruction.

3. (Canceled)

4. (Original) The method of claim 2, wherein said NOP field is inserted at an end of said defining instruction.

5. (Canceled)

6. (Currently Amended) A method for reducing total code size during branching, comprising the steps of

determining a variable latency after a branch instruction for initiating a branch from a first point to a second point in an instruction stream, and
inserting a NOP field into said branch instruction.

7. (Original) The method of claim 6, wherein said branch NOP field is affixed to an end of said branch instruction.

8 (Currently Amended) An apparatus having reduced total code size, comprising a processor including at least one defining instruction followed by at least one using instruction, wherein a latency exists between said at least one defining instruction and said at least one using instruction and wherein at least one of said at least one defining and using instruction includes a NOP field, wherein said NOP field is inserted at an end of said using instruction.

9. (Original) The apparatus of claim 8 wherein said NOP field is inserted into said defining instruction.

1314 10. (Canceled)

11. (Original) The apparatus of claim 9, wherein said NOP field is inserted at an end of said defining instruction.

12. (Canceled)

13. (Currently Amended) An apparatus for reducing total code size during branching, comprising a processor including at least one branch instruction for branching from a first point to a second point in an instruction stream, such that a variable latency exists in the branching between said first point and said second point, and said at least one branch instruction includes a NOP ~~field~~, field.

14. (Original) The apparatus of claim 13, wherein said branch NOP field is affixed to an end of said branch instruction.

15. (Currently Amended) A method for reducing total code size comprising the steps of locating at least one delayed effect instruction followed by NOPs within a code; deleting said NOPs from said code; and inserting a NOP field that specifies the deleted NOPs into a delaying instruction, wherein said deleted NOPs precede said delaying instruction.

16. (Original) The method of claim 15, wherein said delaying instruction is said locating at least one delayed effect instruction.

17. (Canceled)

1316 18. (Original) The method of claim 15, wherein said delayed effect instruction is a load instruction.

19. (Original) The method of claim 15, wherein said delayed effect instruction is a branch instruction.

20. (Currently Amended) An apparatus for reducing total code size comprising a processor including a code containing at least one delayed effect instruction, a delaying instruction including a NOP field that specifies NOPs, wherein said ~~least one of the at least one delayed effect instructions includes a NOP field~~ NOPs precede said delaying instruction.

21. (Original) The apparatus of claim 20, wherein said at least one delayed effect instruction is a load instruction.

22. (Original) The apparatus of claim 20, wherein said at least one delayed effect instruction is a branch instruction.
